

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Assistant Commissioner for Patents
Washington, D.C. 20231-**DC685 U.S. PTO**



Atty. Dkt.: 3842-5

Date: November 20, 2000

Sir:

11/20/00

Attached for filing is the patent application of:

Inventor: JOHNSEN et al

Entitled: **DISTRIBUTED ELECTRONIC DATA PROCESSING**

and including attachments as noted below:

Declaration, Abstract
 11 pages of specification and claims (including 13 numbered claims), and
 13 sheets of accompanying drawing/s.

Record & return the attached assignment to the undersigned.

Priority is hereby claimed under 35 U.S.C 119 based on the following foreign applications, the entire content of which is hereby incorporated by reference in this application:

Application Number	Country	Day/Month/Year Filed
199 5774	Norway	25 November 1999

, respectively.

Certified copy(ies) of foreign application(s) is/are attached.

Please amend the specification by inserting before the first line --This is a _____ of PCT application _____, filed _____, the entire content of which is hereby incorporated by reference in this application.--

Priority is hereby claimed under 35 U.S.C 120/365 based on the following prior PCT applications designating the U.S., the entire content of which is hereby incorporated by reference in this application:

Application Number	Country	Day/Month/Year Filed
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This application is based on the following prior provisional application(s):
Application No. **Filing Date**

respectively, the entire content of which is hereby incorporated by reference in this application, and priority is hereby claimed therefrom.

Please amend the specification by inserting before the first line: --This application claims the benefit of U.S. Provisional Application No. _____, filed _____, the entire content of which is hereby incorporated by reference in this application.--

This application is entitled to "Small entity" status. "Small entity" statement attached.
 The Examiner's attention is directed to the prior art cited in the parent application by applicant and/or Examiner for the reasons stated therein.

Preliminary amendment to claims (attached hereto), to be entered before calculation of the fee below.
 Also attached:

FILING FEE IS BASED ON CLAIMS AS FILED LESS ANY HEREWITH CANCELED

Basic Filing Fee	\$ 710.00
Total effective claims 13 - 20 (at least 20) =	\$ 0.00
Independent claims 2 - 3 (at least 3) =	\$ 0.00
If any proper multiple dependent claims now added for first time, add \$270.00 (ignore improper)	\$ 0.00
SUBTOTAL \$ 710.00	

If "small entity," then enter half (1/2) of subtotal and subtract

Assignment Recording Fee (\$40.00)	\$ 40.00
SECOND SUBTOTAL \$ 710.00	

TOTAL FEE ENCLOSED \$ 750.00	
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Any future submission requiring an extension of time is hereby stated to include a petition for such time extension.
 The Commissioner is hereby authorized to charge any deficiency in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Account No. 14-1140. A duplicate copy of this sheet is attached.

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Signature: H. Warren Burnam, Jr.

JCP12 U.S. PTO
09/714956
11/20/00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

JOHNSEN et al

Atty. Ref.: 3842-5

Serial No. to be assigned

Group: unknown

Filed: November 20, 2000

Examiner: unknown

For: DISTRIBUTED ELECTRONIC DATA PROCESSING

* * * * *

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

PRELIMINARY AMENDMENT

In order to place the above-identified application in better condition for examination, please amend the application as follows:

IN THE CLAIMS

Claim 3, delete "or 2".

Claim 6, change "any one of the previous claims" to -- claim 1 -- .

Claim 7, change "any one of the previous claims" to -- claim 1 -- .

Claim 9, change "any one of the previous claims" to -- claim 1 -- .

Claim 12, delete "or 11".

REMARKS

The above amendments are made to place the claims in a more traditional format.

Respectfully submitted,
NIXON & VANDERHYE P.C.

November 20, 2000

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U.S. PATENT APPLICATION

Inventor(s): Petter JOHNSEN
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Invention: DISTRIBUTED ELECTRONIC DATA PROCESSING

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SPECIFICATION

FIELD OF THE INVENTION.

The invention relates to computer systems comprising two or more processing units (CPU), and in particular to inter process communication in such systems wherein sharing of the workload is accomplished by allocating different processes in a static

5 manner to different CPUs that operate autonomously and with operating systems (OS) that do not include known traditional networking capabilities for such inter process communication across the system.

THE PROBLEM AREAS.

10 In computer systems, meeting the requirements for efficiency and speed can be a problem since a single physical CPU of a typical computer system is only capable of carrying out a single instruction at a time. A commonly employed solution to this problem is to include two or more physical CPUs (or computers) to increase the capacity of the computer system. With more than one CPU in such systems, the various

15 tasks, typically referred to as processes that each would be assigned a unique symbolic process identifier (PID), that essentially comprise the computer programs operated by means of the CPUs, can be distributed among the CPUs to share the workload and to allow that more than one instruction can be carried out at the same time. Typically, in most systems the various processes will need to communicate for different purposes

20 such as information exchange or signals receiving and transmitting, and when different processes are resident of different CPUs, such systems must also include means by which the different processes are allowed to communicate with one another without limiting inter process communication to processes with the same CPU allocation. It should be noted that in such systems it is assumed that the OS or any interrupt routines

25 may also send signals, but only processes can receive signals. When the CPUs or computers of such systems operate autonomously and their OS do not include networking capabilities for "transparent" inter process signals communication across the system, other means for accomplishing inter process communication between processes of different CPUs or computers need to be provided.

30

KNOWN SOLUTIONS AND PROBLEMS WITH THESE.

Several solutions to facilitate inter process communication in multiprocessor or multi-computer systems of the kind mentioned above are known. Some solutions suggest the use of common memory for such communications, while others suggest the addition of

35 other kinds of coupling between the processors in the system.

US Patent no. 5 062 040 discloses a multi-processing arrangement to ensure that signals are not lost and that duplicate signals are not processed, and a multiprocessor system being transparent to existing programs. A signal-handling code fragment is always executed on the processor local to the user portion of an extended process. The user's kernel must send the current signal result (that is, whether a signal has been received which is not being ignored) to a stub process with any stub packet, and any updated signal result must be sent to an active stub process, if any non-ignored signals are subsequently received by the user's process before the stub process responds. This is defined as the pseudo-signal state. Each kernel is arranged to maintain a linked list of table entries which have signals to be sent or forwarded and a system process running at base level that removes signals from the list and forwards them to the correct destination via a communication channel to each processor.

OBJECTS OF THE INVENTION.

Accordingly, it is an object of the present invention to provide an arrangement for inter process communication across a multi-processor system with distributed processing, wherein processor and OS autonomy is maintained and wherein OS common control elements or information is not required.

BRIEF DISCLOSURE OF THE INVENTION.

The above object of the present invention is accomplished by providing a novel virtual link handler (VLH) comprising shadow processes (SP) for actual processes communicating across the system and driver adapters (DA) for communicating CPUs. In an arrangement according to the invention, the symbolic PIDs of resident actual processes of a CPU or computer requiring communication with other resident processes of other CPUs or computers of the system are also defined on such other communicating CPUs or computers, respectively. Accordingly, the symbolic PID of a resident SP of a CPU or computer will be the same as the symbolic PID of a resident actual process of another CPU or computer. Hence, a resident process of a particular CPU, identified by its PID and wishing to communicate a signal to another "remote" resident target process of another "remote" CPU with another PID, will on the CPU on which it resides find a "local" SP with the same symbolic PID as the symbolic PID of the "remote" target process. For exchange of signals, the interface of the local SP to a local communicating actual process appears identical to the interface to actual "remote" target process. The local "SP", however, actually makes no decisions based on the

signal, but serves the function of forwarding the received signal to the other CPU to which the "remote" target process is allocated and is operating on. On the receiving CPU, the signal message is received by a similar SP, which in turn forwards the signal to the actual target process. Accordingly, the communication of signals between CPUs or computers of systems according to the invention is facilitated by means of the novel VLH without requiring that the actual processes have any knowledge of the presence of the VLH. As can be seen from the above standing, the SP may serve to receive from a process a signal for forwarding to another CPU or computer as well as to deliver to a process a signal that has been forwarded from another CPU or computer. To communicate signals between the CPUs, the shadow processes on each CPU have interfaces to driver adapters which in turn have interfaces to drivers for the transmission means that provide the channels of the system used to convey messages from a CPU or computer to another.

15 BRIEF DESCRIPTION OF THE DRAWINGS.

Fig. 1 is a schematic drawing illustrating an example of problem scenario with a system of two CPUs or computers, each with a resident different process requiring to communicate with the other.

Fig. 2 is a schematic drawing illustrating an example of a VLH solution according to the present invention for solving the problem illustrated in fig. 1.

Fig. 3 is a schematic representation of an example of an embodiment of a DA process according to the invention.

Fig. 4 is a schematic representation of an example of an embodiment of a procedure of a driver adapter according to the invention.

25 Fig. 5 is a schematic representation of an example of an embodiment of another procedure of a driver adapter according to the invention.

Fig. 6 is a schematic representation of an example of an embodiment of a shadow process according to the invention.

Fig. 7 is a schematic diagram illustrating a system example with a VLH solution according to the present invention.

30 Fig. 8 illustrates schematically for the system example of fig. 7 the relationship for between the PIDs of actual processes, the PIDs shadow processes of respective the processors and their locations, respectively.

Fig. 9 a-c illustrates schematically for the system example of fig. 7 the development of look-up tables.

Fig. 10 illustrates a transfer of a signal in one direction in the system example of fig. 7.

Fig. 11 illustrates a transfer of a signal in another direction in the system example of fig. 7.

DETAILED DESCRIPTION OF THE EMBODIMENTS.

In the following, by way of examples and with reference to the accompanying drawings, the present invention will be explained in more detail.

10

In fig. 1 is shown an example of a typical problem scenario in a system with two processors and with processes P1 and P2 resident and operating on processors A and B, respectively, wherein the processes wish to communicate. The operating system (OS) of each processor enables communication between processes resident and operating on the same processor, but does not provide for communication with processes resident and operating on different processors. Accordingly, in the typical situation shown in fig. 1, although the processors are provided with physical interconnection for transferring signals, processes P1 and P2 are unable to communicate signals to one another.

15 In fig. 2 is shown a schematic drawing of a similar scenario as shown in fig. 1, but now provided with two new processes P1' and P2', respectively, and driver adapters according to the present invention, to allow signal communication between the processes. In systems wherein the present invention is implemented and wherein different types of processors are utilised, the system designer must take into consideration the use of formats of the various processors, such as byte ordering and padding.

20 With reference to fig. 3, a symbolic representation of an example of an implementation of a DA process according to the invention is shown. After start and initialisation, the process sits in the idle state until a signal event occurs. At signal event, if the signal comes from a driver the course of the process is as indicated by the branch marked (1) below, or, if the signal is to transferred to a driver the course of the process is as indicated by the branch marked (2).

The Receiver () function and the Sender () function are OS functions and return the PID of the receiver and the sender, respectively.

Another system example is shown in fig. 7. It is assumed that the system requirements
 5 have been made such that the required performance of the example can no longer be met by a system comprising an available single processor. Accordingly, to fit the system to available space and processing power, in the system example shown comprising 7 actual processes in total, the actual processes has been divided into two groups (one for each processor). A first group comprising processes P1, P2 and P3 and a second group
 10 comprising processes P4, P5, P6 and P7, are resident and operate on processor A and B, respectively.

Now that the two groups have been separated to be at two different processors, it is needed to re-establish the communication that once was between the processes . This is done, as shown in fig. 8, by introducing and placing "shadow processes" on each
 15 processor, one for each missing "actual" process. The shadow processes are components of the novel VLH which facilitates process signal communication across the system. In the example shown, communication is required between processes P1, P2, P3 of the first group and processes P4, P5, P6 of the second group, respectively. P7 of the second group, however, requires no signal communication with any of the
 20 processes of the first group. Accordingly, there is no need for a shadow process for P7.

After introducing the shadow processes, corresponding systems are established on the processors. With this arrangement, an actual process of the first group can find an addressee for signal communication by a shadow process which correspond to an actual processes of the second group, and vice versa.

25 To allow message communication between the different CPUs, communication means between the two processors are needed. Such communication means could be consisting of drivers and associated physical connections. In order for the shadow processes to make use of such communications means, adapters to the drivers are also needed. The provision of these are also shown in fig. 7.

30

Finally, a way to identify the processes between the processors is required. In the system shown, it is assumed that the processors do not have common memory. According to the invention, the way to identify the processors is shown by the reference table example of fig. 8, corresponding to the system example of fig. 7.

With reference to fig. 8, it can be seen that process P7 of the example does not have a shadow PID or a corresponding PID on processor A as process P7 does not require signals communication with any of the processes residing on processor A.

5

The development of the tables is explained in figs. 9a - 9c. It is assumed that the system does not have common memory, and the reference table of fig. 8 is split into two tables, as shown in fig. 9, and are placed on the respective processors. It can be seen from fig. 9b that process P7 is removed from the table since there is no communication between the processes of processor A and the process P7. Now we have a reference table that makes it possible to tell which process a signal is sent from and to which process a signal is sent.

The system example of fig. 7 is a system with only two CPUs or computers.
 15 Accordingly, in such systems according to the invention with only two CPUs or computers, the address field can be omitted, and the table may be developed further to the table shown for this example in fig. 9c. The reason for this is that a signal sent from an actual process to a SP shall always be forwarded to the other "remote" CPU or computer, and a signal is sent from the DA to a SP shall always be forwarded to an actual "local" process.

Referring to fig. 10, an example of a signal communicated from a process of processor A to a process of processor B is shown. Assume that a signal, S1, is to be sent from actual process P1 to actual process P5. Since the shadow process P5' has the same symbolic PID as the actual process P5, the first recipient of the signal will be the shadow process corresponding to P5, namely P5'. P5' will look up the senders local PID and, if necessary, also its own PID. The shadow process uses these data to look up the corresponding processor independent PID, called the shadow PID. All these data are sent through the lower levels, such as the driver adapter and the driver. At the driver level, it is transmitted to the other processor marked with an ID that tells the driver on the other processor that this is a "shadow process" signal. For the data transmission, retransmissions and/or frame numbering may be utilised, independent of the solution according to the invention. When the signal reaches the driver adapter of the other processor, a look-up is done in the table to find which shadow process corresponds to the sender of the signal. The signal S3 (still carrying the sender and receiver

information) is then sent to that process. That process is in this case P1'. When the signal reaches P1' the sender and receiver information is removed, and the original signal is sent to the process P5 which is the intended receiver.

A signal is sent from P1 to P5 has been explained in the foregoing. As shown in fig. 11,
5 process P5 of the example may respond to the signal of process P1, or a new signal may be sent from P5 to P1. In both cases, the procedure will be similar to the procedure explained in the previous paragraphs, but signals in the example flow in the opposite direction.

It should be noted that signals S2 and S5 may also be a function call into the DA, but is
10 viewed as a signal to show the flow of information.

It should be noted, also, that the response to a signal sent, as described above, is not mandatory in a solution according to the present invention. The two signal sequences described in the foregoing (P1 to P5 and P5 to P1) may therefore be seen as two separate signal sequences.

15

ADVANTAGES

A signal (sometimes called a message) is used by processes to tell other processes something. The OS or any interrupt routines (not explained) may also send signals, but only processes can receive them. This can be accomplished in multiprocessor,
20 distributed systems wherein the OS of each processor does not provide for communication between different processes that in a static manner are resident of and operating on different processors.

Sharing of the workload is accomplished by allocating different processes in a static manner to different CPUs that operate autonomously and with operating systems (OS)
25 that do not include traditional networking capabilities and associated overhead.

The VLH of present invention allows signal exchange between processes resident of and operating on different processors without modifications to a processor dedicated operating system and without adding to system overhead and complexity.

Also, simplicity is maintained by implementing the invention through utilisation of
30 identical shadow processes. Shadow process identities, however, differ.

P a t e n t c l a i m s

1.

An arrangement for inter processor (CPU) or inter computer process signal communication in a system comprising two or more CPUs or computers, wherein CPUs or computers include independent operating systems (OS), inter CPU or computer communications drivers and driver associated interconnections between the CPUs or computers, characterised in a virtual link handler (VLH) comprising at least one shadow process (SP) for each actual process communicating with at least one actual process resident of another CPU or computer and a plurality of driver adapters (DA) each communicating with at least one SP and/or an OS.

2.

The arrangement of claim 1, characterised in that a shadow process associated with a CPU or computer of the system is identified by a process identifier (PID) identical to the PID of the actual process associated with another CPU or computer of the system.

3.

The arrangement of claim 1 or 2, characterised in that a shadow process identifier (SPID) is assigned to each process.

4.

The arrangement of claim 3, characterised in that the SPID itself is a unique process identifier throughout the system.

5.

The arrangement of claim 3, characterised in that the SPID in conjunction with the processor or computer address is a unique process identifier throughout the system.

6.

The arrangement of any one of the previous claims, characterised in that actual processes are statically associated with or residents of particular CPUs or computers of the system.

7.

The arrangement of any one of the previous claims, characterised in that the VLH maintains a reference list of the associations of the actual processes with the respective CPUs or computers of the system.

5

8.

The arrangement of claim 7, characterised in that address tables located at each communicating CPU or computer of the system are developed from the reference list.

10

9.

The arrangement of any one of the previous claims, characterised in that a signal communicated from one process on one CPU or computer to another process on another CPU or computer is temporary modified to include at least the PID of the receiving SP.

15

10.

20

The arrangement of claim 9, characterised in that a signal communicated from one process on one CPU or computer to another process on another CPU or computer is temporary modified to include the PID of the sending SP.

25

11.

The arrangement of claim 1, characterised in that the DA of a CPU or computer is provided with an interface to the SPs and/or OS associated with the same CPU or computer.

25

12.

30

The arrangement of claim 1 or 11, characterised in that the DA of a CPU or computer is provided with an interface to the drivers for CPU or computer interconnections associated with the same CPU or computer.

30

13.

35

A method for inter processor (CPU) or inter computer process signal communication in a system comprising two or more CPUs or computers, wherein CPUs or computers include independent operating systems (OS), inter CPU or inter computer communications drivers and driver associated interconnections between the CPUs or computers,

characterised in the steps of:

- transferring on a CPU or computer a signal intended for another process on another CPU or computer from an originating process to a shadow process representing the other process,
- 5 - amending parameters of the signal by means of the shadow process and a table including the system address of the other process,
- transferring the amended signal to the other CPU or computer by means of driver adapters, the drivers and the driver associated interconnections,
- receiving the amended signal on the other CPU or computer by a shadow process representing the originating process of the signal,
- 10 - amending the received signal by the receiving shadow process by means of parameters carried by the received signal, and
- transferring the amended received signal to the other process for which the signal was intended.

Abstract

In a distributed processing system of two or more interconnected CPUs or computers, each having an operating system, wherein different processes are assigned to particular CPUs in a static manner for workload distribution, a novel virtual link handler (VLH) comprising shadow processes and driver adapters allow processes resident of and operating on a CPU or computer to exchange signals with processes resident of and operating on other CPUs.

(Fig. 2)

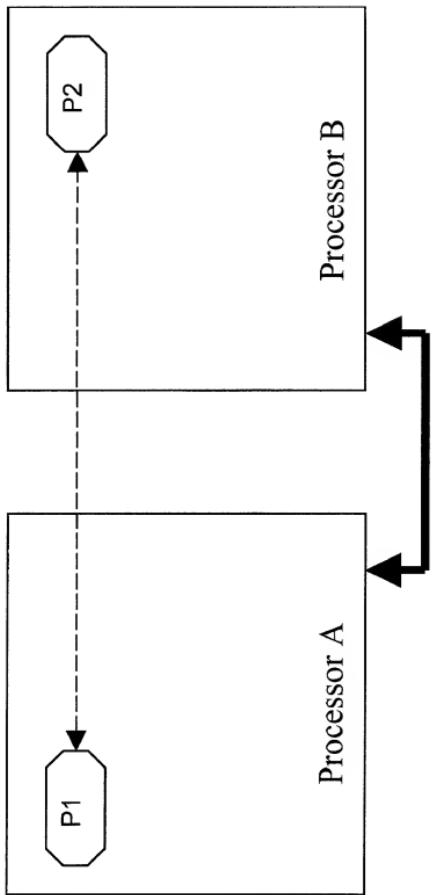


Fig. 1

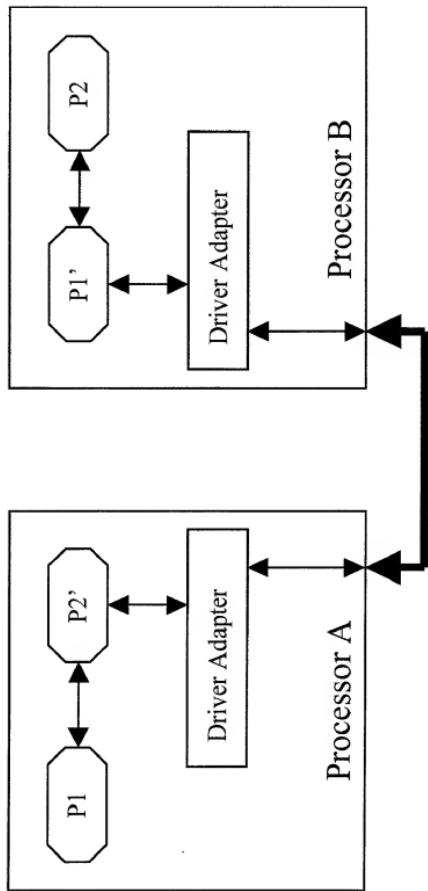


Fig. 2

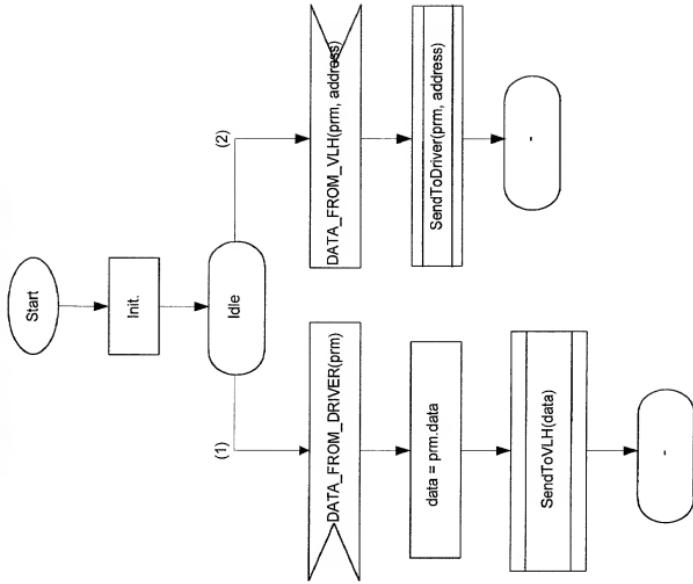


Fig. 3

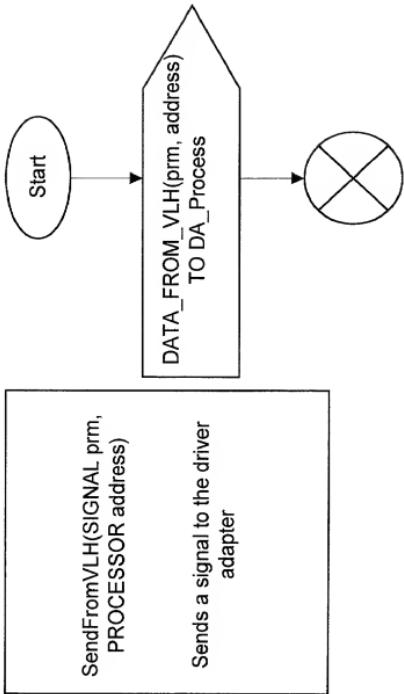


Fig. 4

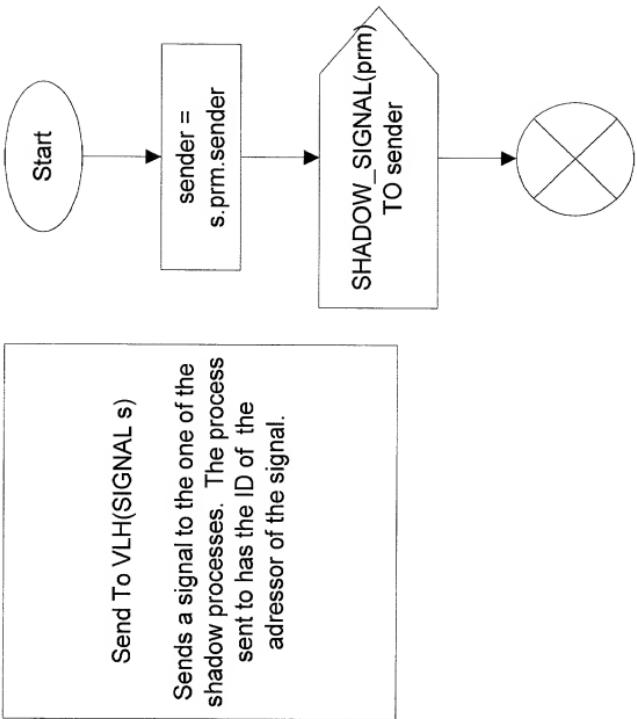
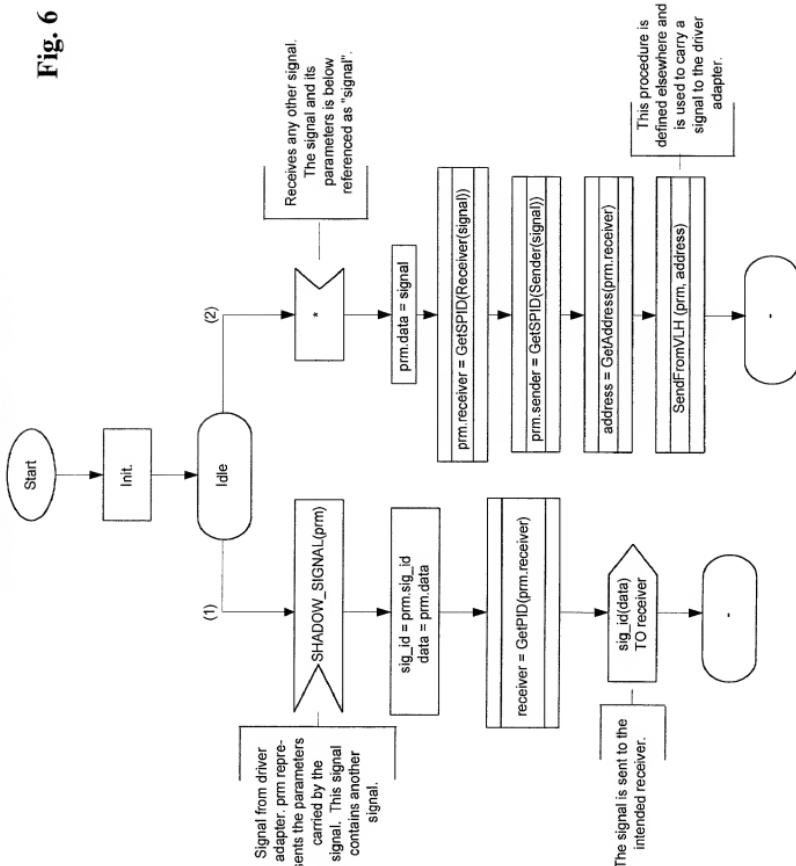


Fig. 5

Fig. 6



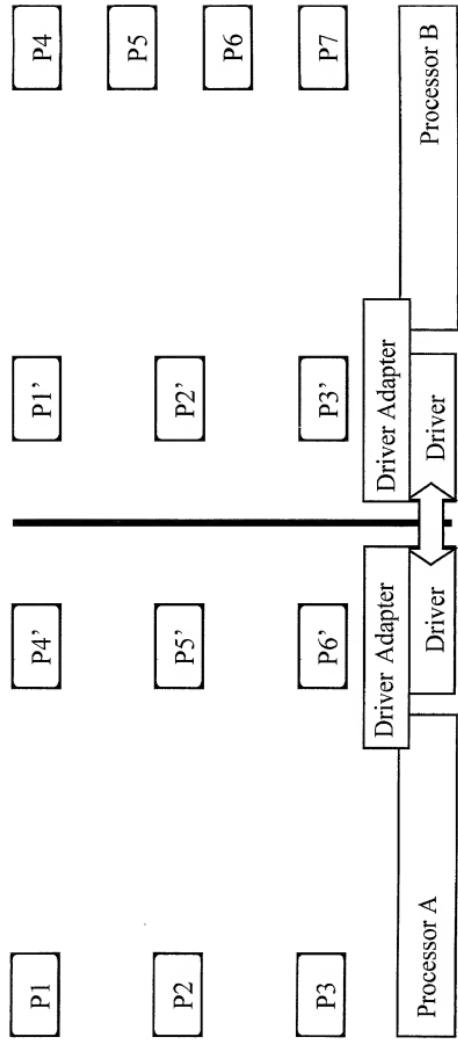


Fig. 7

Fig. 8

Processor A PIDs	Shadow PIDs	Address	Processor B PIDs
P1	sP1	A	P1'
P2	sP2	A	P2'
P3	sP3	A	P3'
P4'	sP4	B	P4
P5'	sP5	B	P5
P6'	sP6	B	P6
-	-	B	P7

Processor A		
PIDs	Shadow PIDs	Address
P1	sP1	A
P2	sP2	A
P3	sP3	A
P4'	sP4	B
P5'	sP5	B
P6'	sP6	B
-	-	-

Processor B		
Address	Shadow PIDs	PIDs
A	sP1	P1'
A	sP2	P2'
A	sP3	P3'
B	sP4	P4
B	sP5	P5
B	sP6	P6
B	-	P7

Fig. 9a

Processor A			Processor B		
PIDs	Shadow PIDs	Address	Address	Shadow PIDs	PIDs
P1	sP1	A	A	sP1	P1'
P2	sP2	A	A	sP2	P2'
P3	sP3	A	A	sP3	P3'
P4'	sP4	B	B	sP4	P4
P5'	sP5	B	B	sP5	P5
P6'	sP6	B	B	sP6	P6

Processor A			Processor B		
PIDs	Shadow PIDs	Address	Address	Shadow PIDs	PIDs
A	sP1	A	A	sP1	P1'
A	sP2	A	A	sP2	P2'
A	sP3	A	A	sP3	P3'
B	sP4	B	B	sP4	P4
B	sP5	B	B	sP5	P5
B	sP6	B	B	sP6	P6

Fig. 9b

Processor A	
PIDs	Shadow PIDs
P1	sP1
P2	sP2
P3	sP3
P4'	sP4
P5'	sP5
P6'	sP6

Processor B	
Shadow PIDs	PIDs
sP1	P1'
sP2	P2'
sP3	P3'
sP4	P4
sP5	P5
sP6	P6

Fig. 9c

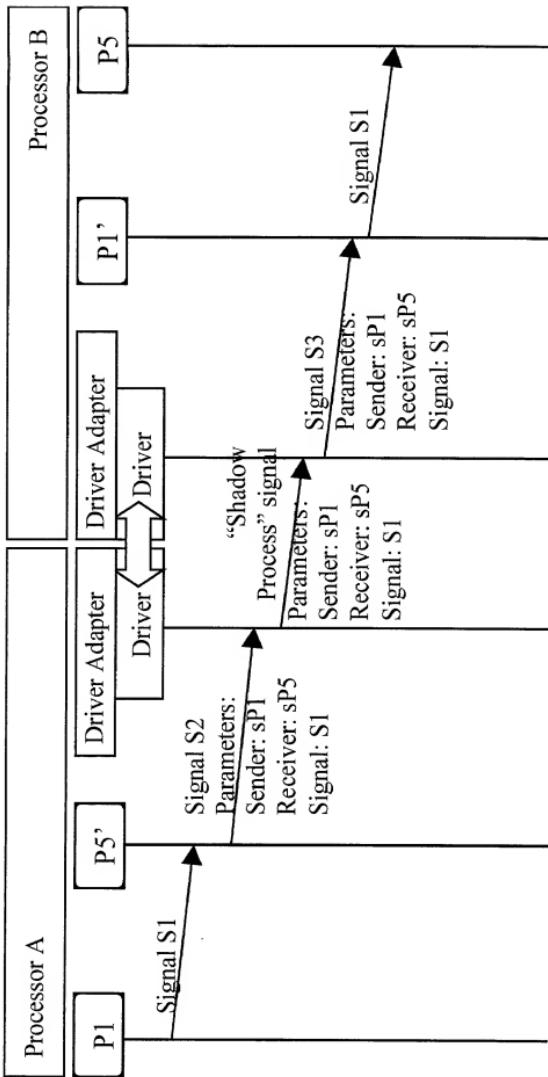


Fig. 10

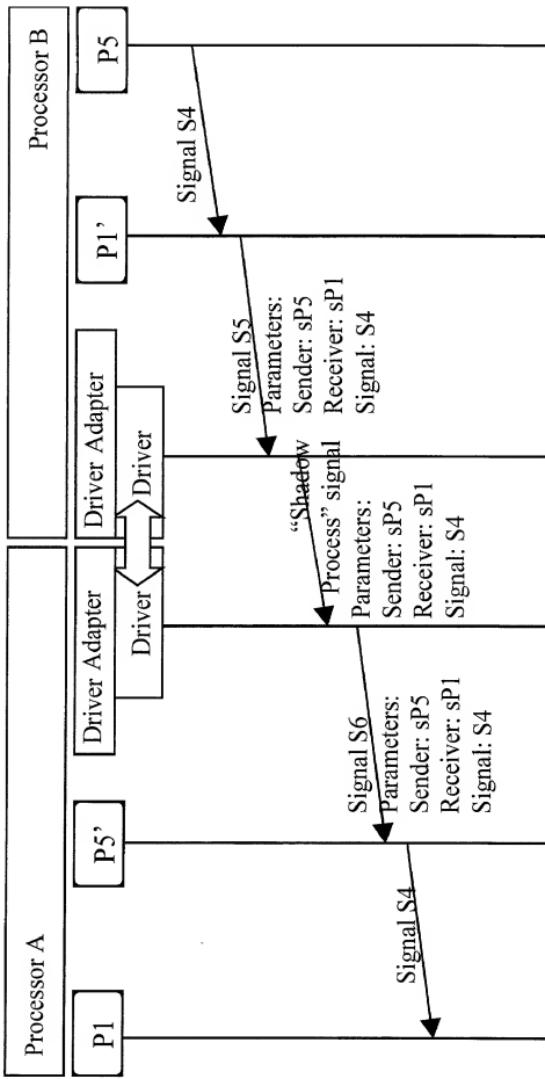


Fig. 11

RULE 63 (37 C.F.R. 1.63)
INVENTORS DECLARATION FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

DISTRIBUTED ELECTRONIC DATA PROCESSING

the specification of which (check applicable box(s)):

is attached hereto
 was filed on _____ as U.S. Application Serial No. _____ (Atty Dkt. No. -)
 was filed as PCT International application No. _____ on _____

and (if applicable to U.S. or PCT application) was amended on _____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. 1.56. I hereby claim foreign priority benefits under 35 U.S.C. 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed or, if no priority is claimed, before the filing date of this application:

Priority Foreign Application(s):

Application Number	Country	Day/Month/Year Filed
19995574	NORWAY	25.11.1999

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below.

Application Number	Date/Month/Year Filed
--------------------	-----------------------

I hereby claim the benefit under 35 U.S.C. 120/365 of all prior United States and PCT international applications listed above or below and, insofar as the subject matter of each of the claims of this application is not disclosed in such prior applications in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. 1.56 which occurred between the filing date of the prior applications and the national or PCT international filing date of this application:

Prior U.S./PCT Application(s): _____ Status: patented
Application Serial No. _____ pending, abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. And on behalf of the owner(s) hereof, I hereby appoint NIXON & VANDERHYE P.C., 1100 North Glebe Rd., 10th Floor, Arlington, VA 22201-4714, telephone number (703) 816-4000 (to whom all communications are to be directed), and the following attorneys thereof (of the same address) individually and collectively owner's/owners' attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent. I also authorize Nixon & Vanderhye to delete any attorney names/numbers no longer with the firm and to act and rely solely on instructions directly communicated from the person, assignee, attorney, firm, or other organization sending instructions to Nixon & Vanderhye on behalf of the owner(s).

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FOR ADDITIONAL INVENTORS, check box and attach sheet with same information and signature and date for each.